

HIGH-PERFORMANCE, SUPERSCALAR-BASED COMPUTER SYSTEM
WITH OUT-OF-ORDER INSTRUCTION EXECUTION

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CROSS-REFERENCE TO RELATED APPLICATIONS

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[0001] This application is a continuation of application Ser. No. 09/436,986, ^{US patent 6,256,720} filed November 9, 1999, now allowed, which is a continuation of application Ser. No. 09/338,563, filed June 23, 1999, now U.S. Patent No. 6,038,654, which is a continuation of application Ser. No. 08/946,078, filed October 7, 1997, now U.S. Patent No. 6,092,181, which is a continuation of application Ser. No. 08/602,021, filed February 15, 1996, now U.S. Patent No. 5,689,720, which is a continuation of application Ser. No. 07/817,810, filed January 8, 1992, now U.S. Patent No. 5,539,911, which is a continuation of application Ser. No. 07/727,006, filed July 8, 1991, now abandoned. Each of the above-referenced applications is incorporated by reference in its entirety herein.

[0002] The present application is related to the following applications, all assigned to the Assignee of the present application:

07/17/97

1. High-Performance, Superscalar-Based Computer System with Out-of-Order Instruction Execution and Concurrent Results Distribution, invented by Nguyen *et al.*, application Ser. No. 08/397,016, filed March 1, 1995, now U.S. Patent No. 5,560,032, which is a continuation of application Ser. No. 07/817,809, filed January 8, 1992, which is a continuation of application Ser. No. 07/727,058, filed July 8, 1991. ^{now abandoned,}

2. RISC Microprocessor Architecture with Isolated Architectural Dependencies, invented by Nguyen *et al.*, application Ser. No. 08/292,177, filed August 18, 1994, now abandoned, which is a continuation of application Ser. No.

now abandoned,

07/817,807, filed January 8, 1992, which is a continuation of application Ser. No. 07/726,744, filed July 8, 1991; *now abandoned*

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3. RISC Microprocessor Architecture Implementing Multiple Typed Register Sets, invented by Garg *et al.*, application Ser. No. 07/726,773, filed July 8, 1991, now U.S. Patent No. 5,493,687;

4. RISC Microprocessor Architecture Implementing Fast Trap and Exception State, invented by Nguyen *et al.*, application Ser. No. 08/345,333, filed November 21, 1994, now U.S. Patent No. 5,481,685, which is a continuation of application Ser. No. 08/171,968, filed December 23, 1993, *now abandoned*, which is a continuation of application Ser. No. 07/817,811, filed January 8, 1992, which is a continuation of application Ser. No. 07/726,942, filed July 8, 1991; *abandoned*, *abandoned*

5. Page Printer Controller Including a Single Chip Superscalar Microprocessor with Graphics Functional Units, invented by Lentz *et al.*, application Ser. No. 08/267,646, filed June 28, 1994, now U.S. Patent No. 5,394,515, which is a continuation of application Ser. No. 07/817,813, filed January 8, 1992, which is a continuation of application Ser. No. 07/726,929, filed July 8, 1991; and *now abandoned*,

6. *now abandoned* Microprocessor Architecture with a Switch Network for Data Transfer between Cache, Memory Port, and IOU, invented by Lentz *et al.*, application Ser. No. 07/726,893, filed July 8, 1991, now U.S. Patent No. 5,440,752.

BACKGROUND OF THE INVENTION

Field of the Invention

[0003] The present invention is generally related to the design of RISC type microprocessor architectures and, in particular, to RISC microprocessor architectures that are capable of executing multiple instructions concurrently.